2023 Digital IC Design Homework 2

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| **Functional Simulation Result** | | |
| **Score** | | **100** |
| (your score message) | | |
| **Description of your design** | | |
| The proposed work is implemented using a finite state machine (FSM) that is divided into four states. The state diagram is described below:  If asynchronous reset is triggered, flow control block will force the state to the IDLE state, or the state will control under the upper diagram. We will give the brief description to the four states.  IDLE: Resets all values and waits for input data.  FETCH\_FIRST: This state splits the number of coming trains and the number of trains.  FETCH: Processes the data and triggers the result flag if it is illegal.  FINISH: Triggers the valid flag so that it can be checked by the testbench. | | |